

Origin and optimization of large dark current increase in InGaAs/InP APD

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Abstract- Dark current of our InGaAs/InP planar SAGCM APD is simulated. Activation energy E_a obtained from the I-V test under temperature range of 240K~300K is cooperated in the simulation. Two origins of the dark current increase of over one order of magnitude from the punchthrough voltage to the breakthrough voltage are analyzed. Our results provide two critical points to reduce the dark current of an InGaAs/InP APD operated under the linear operation mode.

I. INTRODUCTION

In Avalanche Photodiode infrared detectors (APDs), dark current under linear mode has a critical influence on their dark count rate and after pulse characteristics [1]. In our APDs, we observe a dark current increase of over one order of magnitude from the punchthrough voltage (V_p) to the breakthrough voltage (V_b), which has serious affect on the device performance. In this paper, we provide analysis of origins of the dark current increase. Simulation results of I_{TAT} caused by InP multiplication layer trap and I_{GR} caused by InGaAs absorption layer deep level trap according to I-V experiment results under different temperatures reveal that reduction of traps in InP multiplication layer and InGaAs absorption layer and proper optimization of InP charge layer are the critical points to reduce the unexpected dark current.

II. SIMULATION RESULTS

Device A, a typical one of our InGaAs/InP planar SAGCM APD, is the device simulated below. Device B is a comparison device with good dark current characteristics. Fig.1 shows the I-V characteristics of device A and B test results conducted using Keithley 4200. In Fig. 1, we can clearly see the problem of dark

current increasing by about two orders of magnitude from V_p to V_b . The simulations below are aimed at analyzing this problem.

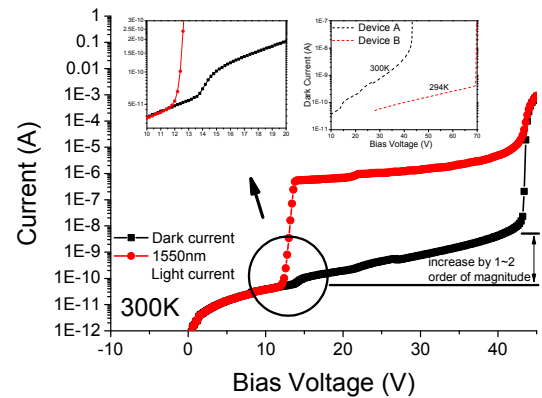


Fig. 1 Experimental I-V characteristics of device A and B

The simulation is conducted in a two dimensional way without the consideration of Guard Ring for simplicity. We solve the coupled Poisson Equation with the Carrier Continuity Equation while components of diffusion current I_{diff} , thermal generation-recombination (GR) current I_{GR} , trap-assisted tunneling (TAT) current I_{TAT} , direct radiative combination current $I_{radiative}$, band to band (B2B) tunneling current I_{B2B} and Auger recombination current I_{Auger} are taken into consideration.

According to the activation energy E_a obtained from the I-V test under temperature range of 240K~300K [2], E_a of is at about $0.25E_g$ of the InP band gap, far away from the mid-band gap. With a high electric field located in the InP multiplication layer, the I_{TAT} overweighs I_{GR} to be the main component of the current resulted from InP multiplication layer traps. Fig. 2 displays the simulated current originated from InP multiplication layer trap and its components (I_{diff} and I_{Auger} are not denoted for they are

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too small compared to the denoted ones). From Fig.2 we can see that the TAT current and GR current match our analysis above, with the proportion of TAT rises with bias voltage approaching V_b where Electric Field is high. Trap level is set to 0.44eV away from the mid-band gap according to the value of fitted activation energy E_a . carrier life time is set to 10 μ s according to an experience value of 0.1 μ s ~100 μ s^[1].

The total current originated from InP multiplication layer trap results in an increase of dark current from the V_p to V_b by over one order of magnitude. However, inset shows that this current is not enough for increasing of dark current. So with the analysis of the current step at V_p , we will provide another origin that contributes to the dark current increase.

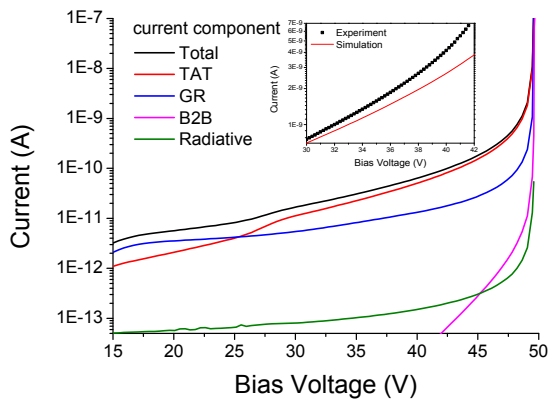


Fig. 2 Simulated current introducing InP multiplication layer trap

Ref.4 suggested that the current step is formed by minority trap in InGaAs absorption layer. Fig. 3 shows our simulated I-V characteristics varying with trap level. Trap concentration is set to $1 \times 10^{14} \text{cm}^{-3}$. Black dash line is the simulated total current shown in Fig. 2. Solid lines denote the net current introduced by InGaAs absorption layer deep level trap.

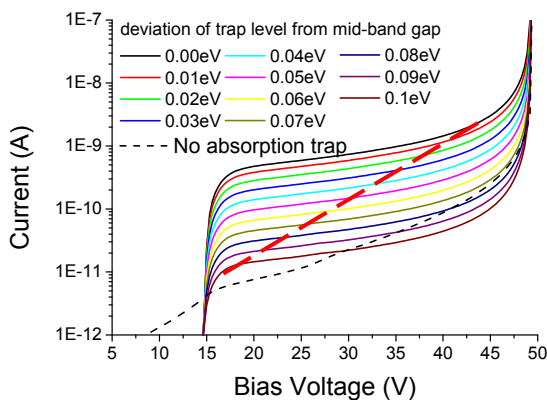


Fig. 3 Simulated I-V characteristics varying with InGaAs absorption layer trap level

Simulation results show that with the increase of trap level deviation from mid-band gap, current step gets lower with an exponential decrease. For the trap concentration of $1 \times 10^{14} \text{cm}^{-3}$, the current reduces by two orders of magnitude when trap level deviation from mid-band gap varies from 0eV to 0.1eV.

Our fitting data shows that the deviation of E_a from InGaAs mid-band gap ($0.75/2=0.375\text{eV}$) varies from 0.005eV to 0.1eV and E_a vs. V_{bias} curve displays linear decreasing characteristic. If we simplify E_a into a minority deep trap level in the InGaAs band gap, the trap level approaches mid-band gap with the bending of energy band which results in an exponential increase of thermal GR current. With trap concentration remaining the same, the current shows over one order magnitude from V_p to V_b (denoted in red dashed line in Fig. 3). A steeper slope of Trap Level vs. V_{bias} curve is related with higher electric field intensity in the InGaAs absorption layer. This suggests a much more proper InGaAs absorption layer electric field adjustment be made by optimizing InP charge layer.

III. CONCLUSIONS

We provided two origins resulting unexpected dark current increase of nearly two orders of magnitude, I_{TAT} caused by InP multiplication layer trap and I_{GR} caused by InGaAs absorption layer deep level trap. Based on the results, we brought up corresponding optimization methods, which include reducing traps in InP multiplication layer and InGaAs absorption layer and reconsidering InP charge layer design on its effect of adjusting InGaAs absorption layer electric field.

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REFERENCES

- [1] Acerbi F, Anti M, Tosi A. Design Criteria for InGaAs/InP Single-Photon Avalanche Diode [J]. IEEE Photonics Journal, 2013, 5(2): 6800209-6800209.
- [2] Cao G, Tang H, Shao X, et al. Performance of extended wavelength InGaAs/InAsP SWIR detector[C]// 7th International Symposium on Advanced Optical Manufacturing and Testing Technologies (AOMATT 2014). 2014.
- [3] Ji X, Liu B, Xu Y, et al. Deep-level traps induced dark currents in extended wavelength $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{InP}$ photodetector[J]. Journal of Applied Physics, 2013, 114(22):224502-224502-5.
- [4] Zeng Q Y, Wang W J, Wen J, et al. Dependence of dark current on carrier lifetime for InGaAs/InP avalanche photodiodes [J]. Optical & Quantum Electronics, 2014, 47(7):1-7.
- [5] Mark A. Itzler, Xudong Jiang, Mark Entwistle, et al. Advances in InGaAsP-based avalanche diode single photon detectors[J]. Journal of Modern Optics, 2009, volume 58(3):174-200.