

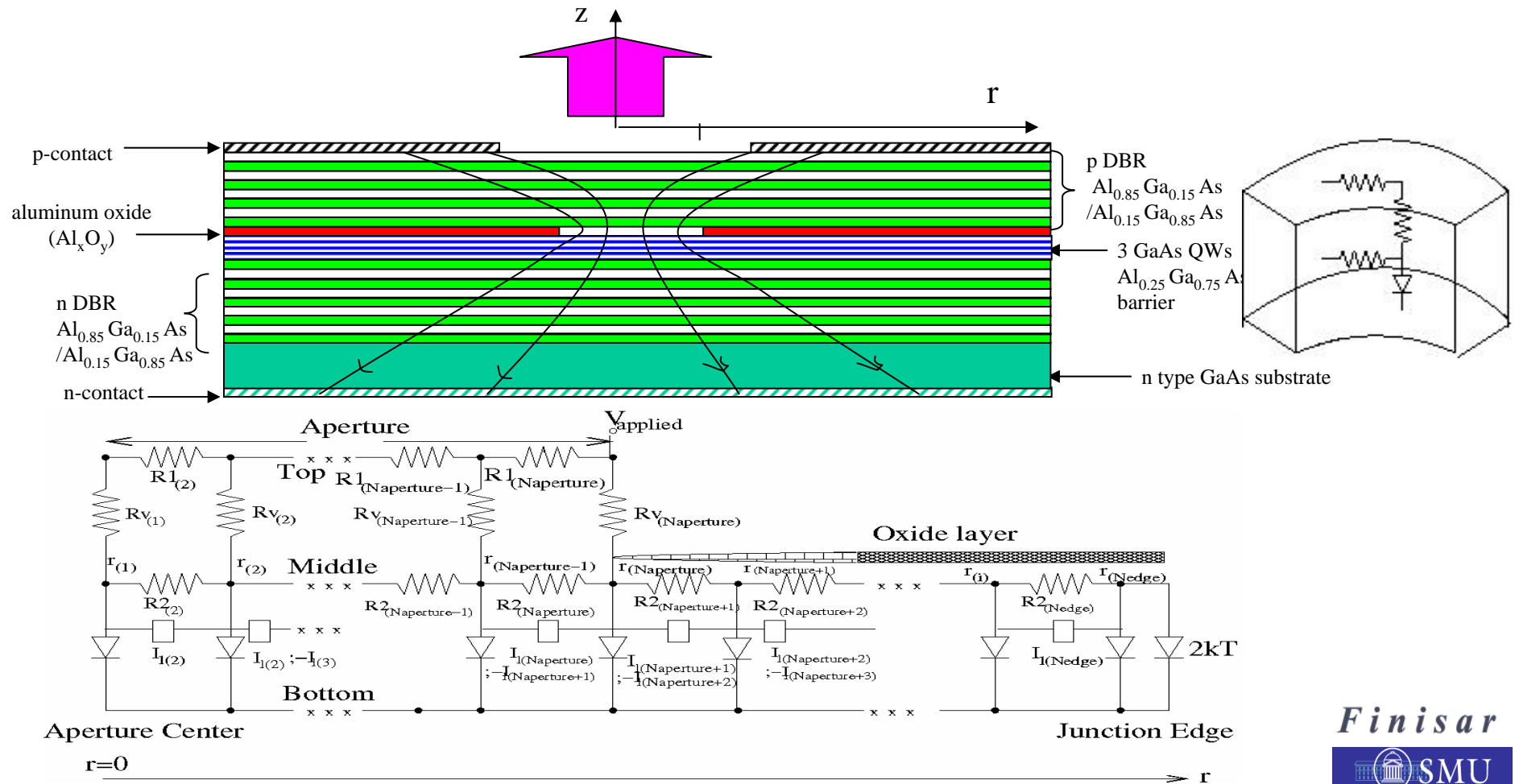
# A Simple Iterative Model for Oxide-Confining VCSELs

Hsueh-hua Chuang<sup>1</sup>, James R. Biard<sup>2</sup>, Jim Guenter<sup>2</sup>, Ralph Johnson<sup>2</sup>, Gary A. Evans<sup>1</sup>, Jerome K. Butler<sup>1</sup>

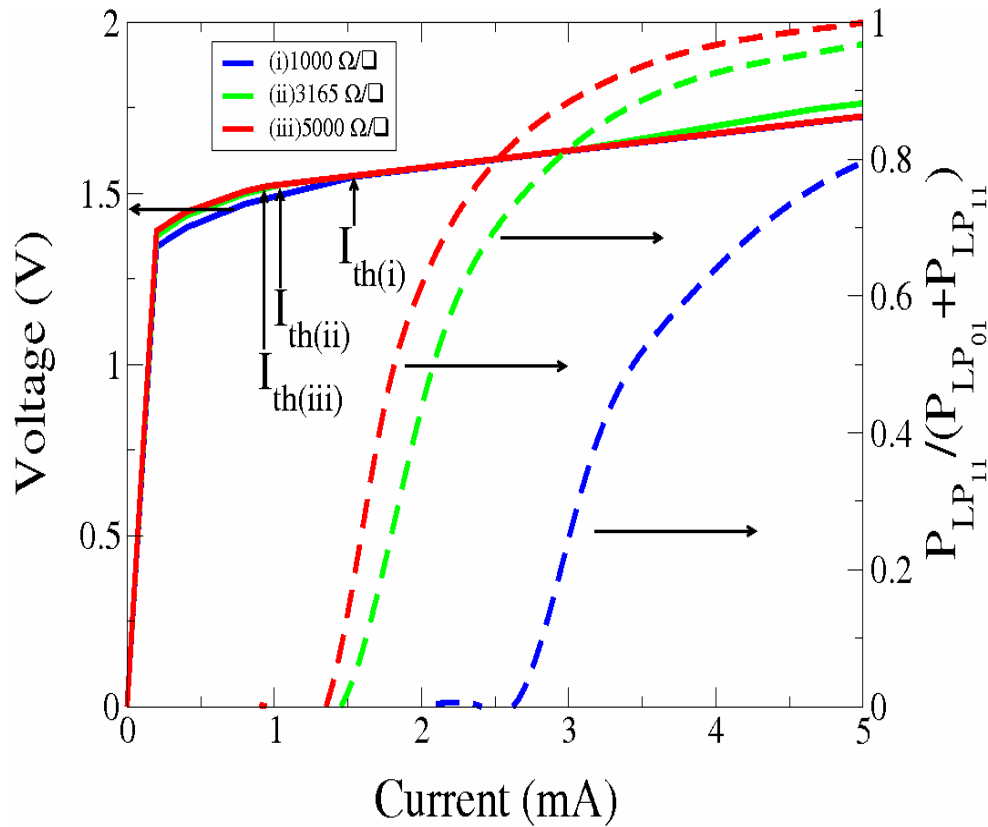
<sup>1</sup>Southern Methodist University, Dallas, TX, <sup>2</sup>Finisar, Allen, TX

email: hchuang@engr.smu.edu

- Empirical model for detailed current and voltage distributions.
- Circuit network to represent the VCSEL.



# Results



- Higher sheet resistance under the oxide layer reduces the threshold – at the expense of allowing a higher order mode at a lower current

- Spatial hole burning (SHB) is primarily related to the p-DBR mirror of VCSELs

